preventing discharge of said parasitic capacitance into the input of said circuit responsive to detection of a negative edge of said input signal, thereby eliminating a need for an additional parasitic capacitance to reduce distortion.--

REMARKS

The present application contains claims 1 through 6, 8, 9 and 11 through 27. Claims 7 and 10 have been canceled without prejudice to Applicant in order to expedite the prosecution of present application. Claims 2, 3, 8, 16, 19 and 23 have been amended. Claims 26 and 27 have been newly added.

The objection to the drawings under 37 CFR. 1.83(a) is hereby respectfully traversed. The recitation "an output device" bridging lines 1 and 2 of claim 2 has been canceled thereby obviating the need for amendment of the drawings. It is therefore requested that this objection be withdrawn.

Claims 19 and 23 have been objected to because the recitation "said introducing step" lacks any antecedent basis. Claims 19 and 23 have been amended to cure this informality and it is submitted this objection should be withdrawn.

Claims 2, 3, 7 through 10, 19 and 20 have been rejected as failing to comply with 35 U.S.C. §112, second paragraph as failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. These claims have been amended, where necessary, in order to comply with the examiner's requirements. More particularly:

The recitation "at input/output device" appearing in claim 2 has been canceled and replaced by "said circuit."

Claims 7 and 10 have been cancelled.

Claim 3 has been amended to recite that the discharge of parasitic capacitance is prevented "into the input of said circuit".

Claim 8 has been amended to delete the word "preventing".

In view of the fact that the above claims have been amended, no further amendment is necessary for claims 9, 19 and 20.

In view of the foregoing, it is submitted that the aforesaid claims now comply with the second paragraph of §112 and that this rejection should be withdrawn.

Claims 1-15 and 18-25 have been rejected under 35 U.S.C. §102(e) as anticipated by Ishikawa et al (Jap. Pat. '430).

Claims 7 and 10 having been canceled, this rejection is respectfully traverse as regards to claim 1-6, 8, 9, 11-15 and 18-25.

Initially, it is noted that the rejection of claims of 1 through 13 based upon Cave et al has been withdrawn; and that the rejection of claims 14 through 17 based on Ooshi has been withdrawn.

Making reference to Japan '430 and referring to any of the figures 1-3 therein, it can be seen that it is imperative to provide **two** (2) parasitic capacitors 3 and 4 in order for the charging/discharging of parasitic capacitor 3 to be ignored. Noting figure 1 in the English

language description thereof, the inventor states that a parasitic capacitor 4 is charged while its discharged by an input/output signal of buffer circuit 6 which responds to changes in the current flowing to the input of J-FET2. According to this description, the voltages of **both poles** of a parasitic capacitor 3 change at the **same phase and level**, allowing the effect of the parasitic capacitor 3 on the input to the FET 2 to be ignored. This technique, however, **absolutely requires** the presence of **second** parasitic capacitor 4.

In the present invention there is no requirement that a second parasitic capacitor be placed in series with the parasitic capacitance of the circuit in order to achieve the desired result. It is further submitted that Japan '430 fails to teach introducing of current to the parasitic capacitance to compensate for the current of the input signal charging the parasitic capacitance. To the contrary, the current is introduced into a **second** parasitic capacitor 4 in the circuit of Japan '430.

With regard to claim 3, the circuitry of Japan '430 likewise fails to prevent discharge of the parasitic capacitance 3. To the contrary, parasitic capacitance 3 is allowed to discharge upon the occurrence of a negative-going edge and charges capacitor 4 which makes up for the reduction of voltage across capacitor 3.

It is further submitted that the Examiner has misinterpreted the teachings of Japan '430 by referring to the field effect transistor (FET) as a detection circuit when in fact the detection circuit is a buffer circuit 6 and not FET 2.

Noting Claim 5, Japan '430 fails to teach diverting current from a parasitic capacitor. To the contrary, when the input signal has a negative-going edge, the circuit 6 of Japan '430 applies a current to the capacitor 4, causing the voltage across capacitor 3 to remain constant, which is clearly different from the circuit and the functions of the circuit of the present invention.

In view of the foregoing, it is submitted that claims 1-6, 8, 9, 11-15 and 18-25 patently distinguish over Japan '430.

Claims 1 through 3, 5, 7, 8, 10 through 13, 18 and 24 have been rejected under 35 U.S.C. §102(b) as anticipated by Bruccoleri et al (488). Claims 7 and 10 having been canceled without prejudice, this rejection is respectfully traversed as regard to claims 1-3, 5, 8, 11-13 and 18-24.

Applicant most respectfully states that the Examiner has incorrectly interpreted the circuitry of the '488 patent which discloses a bi-stable circuit comprised of two (2) cross-coupled invertors INV 1 and INV 2. Although figure 3 of patent '488 shows parasitic capacitance as C_A and C_B, these parasitic capacitances are **not** associated with the inputs of INV 1 and INV 2 but are associated with the nodes A and B. The examiner states that the circuit of figure 3 detects the direction of change of the input voltage an input I+. It is submitted that there is **no** detection circuit for detecting a change in parasitic capacitance in the '488 patent. The capacitances C_{IN} are not described as parasitic capacitances but are referred to as input capacitances, as per column 4, line 19. These parasitic capacitances are

described as being discharged by switches S5 and S6. There is **no** teaching of adjusting for distortion in the bi stable circuit of the '488 patent. This holds true for both the capacitances C_{IN} as well as C_A and C_B.

In view of the foregoing, it is submitted that claims 1-3, 5, 8, 11-13 and 18-24 patentably distinguish over the '488 patent. It is noted that claims 16 and 17 will be allowed upon being rewritten in independent form to include all the limitations of their base claim and any intervening claims. Claim 16 has been amended and is now in independent form, incorporating all of the limitations of claims 14 and 15. In view of the fact that claim 17 depends from amended claim 16, it is submitted that no further amendment to claim 17 is needed.

In view of the foregoing, it is submitted that claims 1-6, 8, 9, 11-15 and 18-25 patentably distinguish over the art of record and reconsideration and allowance of these claims, together with allowable claims 16 and 17, are earnestly solicited.

New claims 26 and 27 further distinguish over the prior art by reciting that the method recited therein "avoids the need for an additional parasitic capacitances" and it is submitted that these claims patentably distinguish over the art of record for the same reasons set forth here and above with regard to original claims 1 and 2 and further distinguish over the art of record in view of the newly added limitations.

Favorable action is awaited.

Respectfully submitted,

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37 CFR §1.111 CLAIM AMENDMENTS - MARKED UP VERSION

2. The method of claim 1, wherein said signal is applied to an input of an [input/output device] said circuit.

3. A method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance, comprising the steps of:

detecting a direction of change in voltage of said input signal; and

preventing discharge of said parasitic capacitance into the input of said circuit responsive to detection of a negative edge of said input signal.

8. Apparatus for reducing distortion of a signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance, comprising:

a detection circuit for detecting a change in voltage of said input signal coupled to said input; and

a correction circuit coupled to said detection circuit for compensating for [preventing] current from said parasitic capacitance to be added to said input signal due to a negative edge of said input signal.

16. Apparatus for reducing distortion of a signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance, comprising:

a first circuit element for selectively providing current to said parasitic capacitance;

a second circuit element for selectively preventing discharge of said parasitic capacitance into said input; and

a control circuit monitoring said input signal for respectively turning on said first circuit element and turning off said second circuit element when a positive going edge of said input signal is detected and for turning off said first circuit element and turning on said second circuit element when a negative going edge of said input signal is detected;

said first and second circuit elements have a common terminal coupled to said parasitic capacitance;

[The apparatus of claim 15 wherein] said first and second circuit elements [are] being transistors.

19. The method of claim 3 wherein the parasitic capacitance is across said input and ground, [said introducing] the step of preventing discharge including introducing the current to said input.

23. The method of claim 13 wherein the parasitic capacitance is across said input and ground, [said introducing] the step of preventing discharge including introducing the current to said input.

Please add the following new claims 26 and 27.

26. A method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance, comprising the steps of:

detecting a direction of change in voltage of said input signal; and

introducing a current to said parasitic capacitance to compensate for current of said input signal charging said parasitic capacitance responsive to detection of a positive edge of said input signal, thereby eliminating a need for an additional parasitic capacitance to reduce distortion.

27. A method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance, comprising the steps of:

detecting a direction of change in voltage of said input signal; and

preventing discharge of said parasitic capacitance into the input of said circuit responsive to detection of a negative edge of said input signal, thereby eliminating a need for an additional parasitic capacitance to reduce distortion.